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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,506	12/12/2003	Seong-Hoon Lee	MIC-42	1009

1473 7590 12/17/2004

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EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,506	LEE, SEONG-HOON	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-16* is/are allowed.

6)☒ Claim(s) *1-12 and 17-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7-19-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4, 9-12, 17-19 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by the Wang et al (U.S. Patent 5,663,665).

Wang et al discloses in figure 4 an apparatus for receiving a reference clock signal CLK IN and outputting clock signals (1...8) having different phases corresponding to said reference clock signal, said circuit comprising a plurality of serially-coupled delay units (D1-8) comprising a first delay unit D1 operative to receive said reference clock signal, said plurality of serially-coupled delay units operative to output clock signals phase-shifted relative to said reference clock signal, each said delay unit of said plurality of serially-coupled delay units providing at least two stages of variable phase adjustment controllable by digital signals (i.e., D1-8 having delay time varied by a control input from filter 40); a phase detector 62 operative to output a signal (32 or 34) indicating a phase difference between said reference clock signal and a clock signal output by said plurality of serially-coupled delay units; and logic circuitry (38 or 40) operative to output digital signals to control phase shifts performed by said plurality of serially-coupled delay units based on said output of said phase detector as required by claim 1.

As to claim 4, it is inherent that outputs D1-D8 having substantially the same frequency since D1-8 are for delaying a signal (i.e., shifting phase).

As to claim 9, figure 4 and 5A show each of D1-8 outputs a corresponding output signals having different phases.

As to claim 10, figure 5A shows plurality of clock signals are phase-shifted by about (360/M) degrees to about 360 degrees relative to said reference clock signal, where M is the number of delay units of said plurality of serially-coupled delays (i.e., TAP1-8 corresponds to D1-8 and they cover one cycle of CLK IN).

As to claim 11, it is inherent that D1-8 are identical to one another since each of them provides the same amount of delay as shown in figure 5A.

As to claim 12, figure 4 shows D1-D8 are control by the same signal derived from filter 40.

As to claims 17-19, they are rejected for reciting a method/step derived from the apparatus recited in claim 1 which is rejected as noted above. It is inherent that a second increment is smaller than the first increment. In an operation of a DLL circuit, an output of a DLL circuit comes closer to a reference signal after completion of each loop. Therefore, phase correction of signal becomes smaller and smaller. In other words, the second increment is less (smaller) than that of the first one.

As to claim 22, the scope of claim is similar to that of claim 1. Therefore, it is rejected for the same reason set forth above. It is noted that each D1-8 has a first stage when a control signal is its initial condition and a second stage when a control signal is not in its initial condition.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Lin reference (U.S. Patent 6,812,753) in view of the Wang et al reference (U.S. Patent 5,663,665).

Lin discloses in figure 6 an apparatus comprising a processor 302; a memory controller 330; plurality of DRAMs (col. 7, lines 2-5) having a DLL circuit as partially required by the claim.

Lin does not disclose a DLL circuit as specifically required by the claim (i.e., specific configuration of DLL recited in claim 23).

Wang et al discloses an apparatus for synchronizing an external clock signal (CLK IN) with a data output (from D1-8) meeting the requirement of a specific configuration of the DLL circuit (See the rejection of claim 1 as noted above).

It would have been obvious to one skilled in the art at the time the invention was made to replace a DLL circuit in Lin with the one taught by Wang et al since a synchronous circuit (i.e., DLL) can be implemented in many different ways in the art.

A skilled artisan in the art would have selected a delay line taught by Wand et al since it is capable of preventing the possibility of a harmonic lock condition from occurring.

5. Claims 2-3, 5-8 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Wang et al reference (U.S. Patent 5,663,665) in view of the Kwak reference (U.S. Patent 6,768,361).

Wang et al discloses all the claimed invention except for teaching a unit delay comprising at least one delay line having an input coupled to an input of said delay unit, said at least one delay line operative to output a first signal having a first phase and a second signal having a second phase; and at least one phase mixer operative to receive said first and said second signals of said at least one variable delay line, said at least one phase mixer operative to output a third signal having a third phase as required by claim 2.

Kwak discloses in figure 4 an apparatus comprising at least one delay unit (10 and 50) having an input EXCLK coupled to the delay unit, at least one delay line 11 operative to output a first signal DCCLK having a first phase and a second signal DCLKE having a second phase (see fig. 6); and at least one phase mixer 50 operative to receive said first and said second signals of said at least one variable delay line, said at least one phase mixer operative to output a third signal having a third phase INCLK (see fig. 6) as required by claim 2.

It would have been obvious to one skilled in the art at the time the invention was made incorporate the teachings of Kwak into that of Wang et al since a delay unit is known to be implemented in many different ways in the art.

A skilled artisan in the art would have selected the teachings of Kwak since the clock signal derived from Kwak's invention would be independent from jitter elements.

As to claim 3, figure 6 shows the third phase is in between the first and the second phases.

As to claim 5, fig. 4 shows the variable delay line 10 as required by the claim.

As to claims 6 and 8, fig. 4 shows the variable delay line 10 comprising two variable delay lines 11 and 12, namely coarse and fine delays.

As to claim 7, fig. 4 shows the variable delay line 10 comprising phase mixer 50.

As to claims 20 and 21, they are rejected for reciting method/step derived from the apparatus of claims 2 and 8, which are rejected above.

Allowable Subject Matter

6. Claims 13-16 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose an apparatus comprising elements being configured as recited in claims. Specifically, none of the prior art teaches or fairly suggests, among other things, the limitation "*two parallel phase mixer each operative to receive the output signals from the two parallel delay lines, the two phase mixer each operative to output a signal having a phase between the phases of the delay line output signals, and a third phase mixer operative to receive the output signals from the two parallel phase mixers*" as required by claim 13.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
12-11-04 ATL

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